



RISE KRISHNA SAI PRAKASAM GROUP OF INSTITUTIONS:: ONGOLE

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AN ISO 9001:2015 Certified Institute

Department of Electronics and Communication Engineering

Report on

Guest lecture

“Micro, Nano Scale Technology and Beyond”

Resource person

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On

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Guest Lectures were conducted in ECE Department on **05.01.2019**. The program started at **10 A.M** with inauguration. The Guest speakers for the session were **Dr. Kodali Prakash**, Assistant Professor, Department of Electronics and Communication Engineering, National Institute of Technology, Warangal - 506004, Telangana, INDIA. The topic was **“Micro, Nano Scale Technology and Beyond”**. He started the lecture from invention of the ICs, introduced how Moore’s law satisfied the present scenario of IC fabrications. Basics of Transistors, Need for MOS transistors, FPGA, SOC Architectures, Generation of ICs, Scope and Future of VLSI were discussed. The target audience for the session was II, III and IV year ECE students.

Nanotechnology is simply science and engineering carried out on the nanometer scale, that is, 10^{-9} meters. In the last two decades, researchers began developing the ability to manipulate matter at the level of single atoms and small groups of atoms and to characterize the properties of materials and systems at that scale. This capability has led to the astonishing discovery that clusters of small numbers of atoms or molecules—nanoscale clusters—often have

properties (such as strength, electrical resistivity and conductivity, and optical absorption) that are significantly different from the properties of the same matter at either the single-molecule scale or the bulk scale.

He focused on circuit design and the techniques used to minimize capacitive and inductive noise. He also introduced how to integrate analog circuits on large digital chips presents significant challenges, primarily due to substrate noise coupling. He also summarized that CMOS processes move into the nanoscale—that is, less-than-12-nm—range, it becomes increasingly difficult to maintain the energy efficiency for medium- to high-accuracy analog circuits, Accuracies may decrease as the technology scales down. Analog-chip designers can improve energy efficiency using different approaches, from selecting the optimum CMOS technology to clever system-level design. He also shown the devices he manufactured in his research lab.





His current research interest is Printed Flexible Electronics, Embedded Systems, VLSI - Nano Electronics, Signal Conditioning Circuits& Systems and Biomedical Electronics. He also suggested the future scope and research avenues availed in this domain.